16.265 Logic Design Laboratory Grade Sheet

This page should be stapled together with the rest of the report. After the grading, this page will be taken and kept by the TAs for the record.

1. (This section to be completed by student)

Student logic number: 146

Student name: (Last) VO, (first) PHONG

Experiment number: 2

Date/time: 3/ 09 / 2018, 12 p.m.

1. Preliminary checking
2. Is the report written on 8½” x 11” paper and stapled at left margin?
3. Is a cover page included?
4. Is the report written using the given template?
5. Is the correct assignment used in design?

Report will not be accepted if the answer is “NO” to any of the above questions.

1. Grade

1. Design procedures: supporting theory, details, etc. (25) \_\_\_\_\_\_\_\_\_\_\_

2. Is design correct? (50) \_\_\_\_\_\_\_\_\_\_\_

3. Minimization of design (15) \_\_\_\_\_\_\_\_\_\_\_

5. List of ICs and unused gates (10) \_\_\_\_\_\_\_\_\_\_\_

Gross grade (100) \_\_\_\_\_\_\_\_\_\_

1. Adjustment to gross grade

1. Grade sheet, cover page (5) \_\_\_\_\_\_\_\_\_\_\_

2. Title box of schematic diagram (5) \_\_\_\_\_\_\_\_\_\_\_

3. Schematic diagram in correct format (10) \_\_\_\_\_\_\_\_\_\_\_

4. Misrepresentation of test (simulation) results (30) \_\_\_\_\_\_\_\_\_\_\_

1. 5. Neatness and legibility (10) \_\_\_\_\_\_\_\_\_\_
2. 6. Templates (20) \_\_\_\_\_\_\_\_\_\_

Final grade (100) \_\_\_\_\_\_\_\_\_\_

Comments: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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Grader: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Date: \_\_\_\_/\_\_\_\_/\_\_\_\_\_\_\_\_

|  |  |
| --- | --- |
| 16.265 Logic Design | |
| Student Logic Number | 146 |
| Name | PHONG VO |
| E-mail address (print) | Phong\_Vo@student.uml.edu |
| Experiment Number | 2 |
| Date | 3/9/2018 |

|  |  |
| --- | --- |
| For grader use | |
|  |  |
| Schematic diagram submitted is different from the one in the report. (Need to re-submit the schematic diagram in the report or will be graded based on a maximum of 50 points.) | 5 points deduction |
| Cannot open file |  |
| File is not readable |  |
| Date student is notified to re-submit a schematic file by e-mail |  |
| Date schematic file received |  |

Report will be graded based on a maximum of 50 (out of 100 points) if a schematic diagram is not received within three calendar days of notification or the re-submitted schematic file still cannot be opened or is not readable.

Grade: \_\_\_\_\_\_\_\_\_\_\_

Experiment 2 Design of a Code Converter

1. Input and output code assignment

Input code: Reflected code 1

#### Output code: (5,4,-1,-2) code

2. Design Procedures

### Truth table for code converter (If ABCD is an invalid input code,

### write “invalid” in the column for decimal digits.)

|  |  |  |  |
| --- | --- | --- | --- |
| Decimal  digit for binary code | Decimal equivalent of ABCD | Inputs A B C D | Outputs  V W X Y Z |
| 4 | 0 | 0 0 0 0 | 1 0 1 0 0 |
| 3 | 1 | 0 0 0 1 | 1 1 0 0 1 |
| 1 | 2 | 0 0 1 0 | 1 0 1 1 1 |
| 2 | 3 | 0 0 1 1 | 1 0 1 0 1 |
| invalid | 4 | 0 1 0 0 | 0 d d d d |
| invalid | 5 | 0 1 0 1 | 0 d d d d |
| 0 | 6 | 0 1 1 0 | 1 0 0 0 0 |
| invalid | 7 | 0 1 1 1 | 0 d d d d |
| 5 | 8 | 1 0 0 0 | 1 1 0 0 0 |
| 6 | 9 | 1 0 0 1 | 1 1 1 1 1 |
| 8 | 10 | 1 0 1 0 | 1 1 1 1 0 |
| 7 | 11 | 1 0 1 1 | 1 1 1 0 1 |
| invalid | 12 | 1 1 0 0 | 0 d d d d |
| invalid | 13 | 1 1 0 1 | 0 d d d d |
| 9 | 14 | 1 1 1 0 | 1 1 1 0 0 |
| invalid | 15 | 1 1 1 1 | 0 d d d d |

Express V, W, X, Y, Z in minterm list form

V = Σ m(0,1,2,3,6,8,9,10,11,14)

W = Σ m(1,8,9,10,11,14) + d(4,5,7,12,13,15)

X = Σ m(0,2,3,9,10,11,14) + d(4,5,7,12,13,15)

#### Y = Σ m(2,9,10) + d(4,5,7,12,13,15)

Z = Σ m(1,2,3,9,11) + d(4,5,7,12,13,15)

### Design for V

### K-map for V

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB CD | 00 | 01 | 11 | 10 |
| 00 | 1 | 0 | 0 | 1 |
| 01 | 1 | 0 | 0 | 1 Simplest SOP = B’ + CD’ |
| 11 | 1 | 0 | 0 | 1 |
| 10 | 1 | 1 | 1 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB CD | 00 | 01 | 11 | 10 |
| 00 | 1 | 0 | 0 | 1 |
| 01 | 1 | 0 | 0 | 1 Simplest POS = (B’+C)(B’+D’) |
| 11 | 1 | 0 | 0 | 1 |
| 10 | 1 | 1 | 1 | 1 |

Realization and gate transformation for V

Minimize either the simplest SOP or the simplest POS obtained from the K-map to an expression with a minimum number of literals.

V = B’ + CD’

Draw the circuit for V with a minimum number of 2-input AND gates and 2-input OR gates using LogicWorks:

### Insert circuit diagram below



### Draw the circuit for V with only NAND gates and/or NOR gates using LogicWorks:

### Insert circuit diagram below



### Design for W

### K-map for W

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB CD | 00 | 01 | 11 | 10 |
| 00 | 0 | d | d | 1 |
| 01 | 1 | d | d | 1 Simplest SOP = AB’ + C’D + AC |
| 11 | 0 | d | d | 1 |
| 10 | 0 | 0 | 1 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB CD | 00 | 01 | 11 | 10 |
| 00 | 0 | d | d | 1 |
| 01 | 1 | d | d | Simplest POS = (A+D)(A+C’) 1 |
| 11 | 0 | d | d | 1 |
| 10 | 0 | 0 | 1 | 1 |

Realization and gate transformation for W

Minimize either the simplest SOP or the simplest POS obtained from the K-map to an expression with a minimum number of literals.

W = (A+D)(A+C’) = A + C’D

Draw the circuit for W with a minimum number of 2-input AND gates and 2-input OR gates using LogicWorks:

### Insert circuit diagram below



### Draw the circuit for W with only NAND gates and/or NOR gates using LogicWorks:

### Insert circuit diagram below



### Design for X

### K-map for X

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB CD | 00 | 01 | 11 | 10 |
| 00 | 1 | d | d | 0 |
| 01 | 0 | d | d | Simplest SOP =A’C’D’ + AB + AD + CD + AC + B’C 1 |
| 11 | 1 | d | d | 1 |
| 10 | 1 | 0 | 1 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB CD | 00 | 01 | 11 | 10 |
| 00 | 1 | d | d | 0 |
| 01 | 0 | d | d | Simplest POS = (A’+C+D)(A+C+D’)(A+B’) 1 |
| 11 | 1 | d | d | 1 |
| 10 | 1 | 0 | 1 | 1 |

Realization and gate transformation for X

Minimize either the simplest SOP or the simplest POS obtained from the K-map to an expression with a minimum number of literals.

### X = (A’+C+D)(A+C+D’)(A+B’) = [C+(A’+D)(A+D’)](A+B’) = (C+A’D’+AD)(A+B’)

Draw the circuit for X with a minimum number of 2-input AND gates and 2-input OR gates using LogicWorks:

### Insert circuit diagram below



### Draw the circuit for X with only NAND gates and/or NOR gates using LogicWorks:

### Insert circuit diagram below



### Design for Y

### K-map for Y

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB CD | 00 | 01 | 11 | 10 |
| 00 | 0 | d | d | 0 |
| 01 | 0 | d | d | Simplest SOP == AB’C’D + A’B’CD’ + AB’CD’= B’(AC’D + A’CD’ + ACD’)= B’(AC’D + CD’) 1 |
| 11 | 0 | d | d | 0 |
| 10 | 1 | 0 | 0 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB CD | 00 | 01 | 11 | 10 |
| 00 | 0 | d | d | 0 Simplest POS= (C+D)B’(A+D’)(C’+D’)= (C+D)B’(D’ + AC’)= B’(CD’ + AC’D) |
| 01 | 0 | d | d | 1 |
| 11 | 0 | d | d | 0 |
| 10 | 1 | 0 | 0 | 1 |

Realization and gate transformation for Y

Minimize either the simplest SOP or the simplest POS obtained from the K-map to an expression with a minimum number of literals.

Y = B’(CD’ + AC’D)

Draw the circuit for Y with a minimum number of 2-input AND gates and 2-input OR gates using LogicWorks:

### Insert circuit diagram below



### Draw the circuit for Y with only NAND gates and/or NOR gates using LogicWorks:

### Insert circuit diagram below

### Design for Z

### K-map for Z

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB CD | 00 | 01 | 11 | 10 |
| 00 | 0 | d | d | 0 |
| 01 | 1 | d | d | Simplest SOP = D + A’B’C 1 |
| 11 | 1 | d | d | 1 |
| 10 | 1 | 0 | 0 | 0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB CD | 00 | 01 | 11 | 10 |
| 00 | 0 | d | d | 0 |
| 01 | 1 | d | d | 1 Simplest POS = B’(C+D) (A’+C’+D) |
| 11 | 1 | d | d | 1 |
| 10 | 1 | 0 | 0 | 0 |

Realization and gate transformation for Z

Minimize either the simplest SOP or the simplest POS obtained from the K-map to an expression with a minimum number of literals.

Z = D + A’B’C

Draw the circuit for Z with a minimum number of 2-input AND gates and 2-input OR gates using LogicWorks:

### Insert circuit diagram below



### Draw the circuit for Z with only NAND gates and/or NOR gates using LogicWorks:

### Insert circuit diagram below



4. List of ICs and unused gates

|  |  |  |  |
| --- | --- | --- | --- |
| IC number | Type number | Function | Unused gates |
| 1 | 7400 | Quad 2-input NAND | 0 |
| 2 | 7400 | Quad 2-input NAND | 0 |
| 3 | 7400 | Quad 2-input NAND | 0 |
| 4 | 7400 | Quad 2-input NAND | 1 |
| 5 | 7400 | Quad 2-input NAND | 0 |
| 6 | 7402 | Quad 2-input NOR | 0 |
| 7 | 7402 | Quad 2-input NOR | 1 |
| 8 | 7402 | Quad 2-input NOR | 4 |

### 5. Simulation results

### Table for simulation results

(Place a check mark in the column “Incorrect results” for each simulation value that is different from the value listed in the truth table in Section 2.)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Decimal  digit | Inputs | Simulation results | | Incorrect results | | | | |
| A B C D | V | W X Y Z | V | W | X | Y | Z |
| 0 | 0 1 1 0 | 1 | 0 0 0 0 |  |  |  |  |  |
| 1 | 0 0 1 0 | 1 | 0 1 1 1 |  |  |  |  |  |
| 2 | 0 0 1 1 | 1 | 0 1 0 1 |  |  |  |  |  |
| 3 | 0 0 0 1 | 1 | 1 0 0 1 |  |  |  |  |  |
| 4 | 0 0 0 0 | 1 | 0 1 0 0 |  |  |  |  |  |
| 5 | 1 0 0 0 | 1 | 1 0 0 0 |  |  |  |  |  |
| 6 | 1 0 0 1 | 1 | 1 1 1 1 |  |  |  |  |  |
| 7 | 1 0 1 1 | 1 | 1 1 0 1 |  |  |  |  |  |
| 8 | 1 0 1 0 | 1 | 1 1 1 0 |  |  |  |  |  |
| 9 | 1 1 1 0 | 1 | 1 1 0 0 |  |  |  |  |  |
| Invalid input code | 0 1 0 0 | 0 | 0 0 0 0 |  | Recoding of WXYZ for invalid input codes not required | | | |
| Invalid input code | 0 1 0 1 | 0 | 1 0 0 1 |  |
| Invalid input code | 0 1 1 1 | 0 | 0 0 0 1 |  |
| Invalid input code | 1 1 0 0 | 0 | 1 0 0 0 |  |
| Invalid input code | 1 1 0 1 | 0 | 1 1 0 1 |  |
| Invalid input code | 1 1 1 1 | 0 | 1 1 0 1 |  |

6. Schematic diagram

### Schematic diagram for the 4-input 5-output circuit

Attach a complete schematic diagram including the title box.